A New CMOS Current Reference with High Order Temperature Compensation

ZHOU Hao, ZHANG Bo, LI Zhao-ji, LUO Ping
School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China  Chengdu  610054  China

Abstract  A new high order CMOS temperature compensated current reference is proposed in this paper, which is accomplished by two first order temperature compensation current references. The novel circuit exploits the temperature characteristics of integrated-circuit resistors and gate-source voltage of MOS transistors working in weak inversion. The proposed circuit, designed with a 0.6 μm standard CMOS technology, gives a good temperature coefficient of 31ppm/°C [−50–100°C] at a 1.8V supply, and also achieves line regulation of 0.01%/V and –120dB PSR at 1 MHz. Comparing with other presented work, the proposed circuit shows better temperature coefficient and Line regulation.

Key words  current reference;  temperature-compensation;  weak inversion;  poly resistor

The current mode approach in circuit design is becoming more common, because circuits designed using this approach will always work at higher speed than its voltage mode counterpart. However, the accuracy of current mode circuits strongly depends on temperature stability of current reference. In voltage mode, we can use bandgap circuit or CMOS voltage reference to ensure correct standard over a wide temperature range. But conventional current reference is only addition of a PTAT (Proportional to Absolute Temperature) and IPTAT (Inverse Proportional to Absolute Temperature) current [1-4], which could not have good temperature coefficient only with first order temperature compensation. The principle of conventional compensation is showed in Fig.1. A new high order temperature compensation method is described in this paper, which is shown in Fig.2. The basic principle is adding a properly scaled curved-down first order temperature compensation current $I_{ref1}$ to a properly scaled curved-up first order temperature compensation current $I_{ref2}$, finally, the high order curvature correction current $I_{REF}$ is optimized by the appropriated ratio of $a/b$. Comparing with presented works, the proposed circuit shows a better temperature stability with little penalty in the circuit complexity due to the new compensation technique employed. Most of important, in traditional current reference design, the temperature coefficients (tempco) of integrated resistors are boring monsters, just the reverse, in the proposed circuit based on MOS transistors working in weak inversion, the tempcos of resistors are well utilized.

$V_{GS}$ versus Temperature in Weak Inversion

For MOS transistors, the gate-source voltages less than the threshold voltage but high enough to create a depletion region at the surface of the silicon, the device
operates in weak inversion (subthreshold region)\(^5\), the gate-source voltage for MOS in weak inversion has been given by\(^6\):

\[
V_{GS}(T) = V_{FB} + E_G + \frac{V_{GS}(T_o) - V_{FB} - E_G}{T_o} - \frac{nKT}{q} (\alpha + \gamma - 2) \ln \frac{T}{T_o}
\]

(1)

where \(E_G\) is the silicon bandgap energy, \(K\) is the boltzmann’s constant, \(q\) is the charge of an electron, \(n\) is subthreshold slope factor, \(V_{FB}\) is flat band voltage, \(\gamma\) models the temperature dependence of carriers’ mobility and \(T_0\) is the reference temperature, the drain current \(I_{D}\) is proportional to \(T\) near \(T_0\):

\[
I_{D}(T) = I_{D}(T_0) \left[ 1 - \lambda (T - T_0) \right]
\]

For typical values of parameters above, \(A>0, B>0\), the voltage \(V_{GS}\) decreases with temperature.

2 Implementation of the Current Reference

The proposed current reference shown in Fig 3 is composed of four sub-circuits. The first consists of transistors M1-M4, resistors \(R_0-R_2\), the op-amp OP1 and frequency compensation capacitor to generate \(I_{ref1}\). The second includes transistors M5-M11, resistors \(R_3-R_5\), the op-amp OP2 and frequency compensation capacitor to give \(I_{ref2}\). The third is current superposition circuit consisting of \(M5-M7\) to output \(I_{REF}\). The fourth is start-up circuit composed of \(M8-M9\), \(R_6-R_8\). The OP1 and OP2 architectures are the P-channel input folded-cascode configuration shown in Fig.4 to increase the common mode input range and to improve the power supply rejection\(^7\) (\(PSR = \Delta I_{REF}/\Delta V_{DD}\)) performance of the current reference.

In the first sub-circuit, \(M1\) and \(M2\) operate in weak inversion, \((W/L)_1/(W/L)_2 = 1\), \((W/L)_3/(W/L)_4 = N > 1\), the voltage across \(R_0\) is given by\(^9\):

\[
V_{R_0} = V_T \ln N
\]

(3)

For the OP1 forces the drains of \(M1\) and \(M4\) to be at the same potentials and the resistance of \(R_1\) and \(R_2\) are nominal equal, \(I_{ref1}\) can be given by

\[
I_{ref1} = \frac{V_{GS}(T)}{R_1(T)} + \frac{V_T \ln N}{R_2(T)}
\]

(4)

In the design, \(R_1\) and \(R_2\) are implemented by negative tempco material such as high resistive poly resistor, \(R_0\) is implemented by positive tempco material such as low resistive poly resistor\(^8\-\(^9\)). They can be written as

\[
R_i(T) = R_i(T_o) \left[ 1 - \lambda_i (T - T_0) \right]
\]

(5)

where \(-\lambda_1\) and \(\lambda_2\) are tempcos of resisters.

Now Eq.(4) can be expressed as

\[
I_{ref1} = \frac{A - BT}{R_i(T_o)} \left[ 1 - \lambda_i (T - T_0) \right] + \frac{V_T \ln N}{R_2(T_o)} \left[ 1 + \lambda_2 (T - T_0) \right]
\]

(7)

If Taylor expansions at \(T = T_0\) are performed on \([1-\lambda_i(T - T_0)]\), \([1+\lambda_2(T - T_0)]\) and omit high order terms, we obtain

\[
I_{ref1} = \frac{A - BT}{R_i(T_o)} [1 + \lambda_i (T - T_0)] + \frac{V_T \ln N}{R_2(T_o)} [1 - \lambda_2 (T - T_0)]
\]

(8)

If the ratio of \(R_2(T_o)/R_2(T_0)\) is \(m_1\) to make \(dI_{ref1}/dT = 0\) at \(T = T_0\), then the 1st order temperature compensation current is achieved, \(m_1\) should satisfies

\[
\begin{align*}
R_2(T_o)/R_2(T_0) &= m_1 \\
V_{R_0} &= V_T \ln m_1
\end{align*}
\]
Further insight is gained by differentiating Eq.(8) with respect to \( T \), and yields the coefficient of \( T^2 \) in \( I_{ref1} \):

\[
\frac{d^2 I_{ref1}}{dT^2} = -2(B\lambda_n + m\lambda_1 \frac{K}{q} \ln N)
\]

(10)

For typical values of \( B \), \( \lambda_n \), \( \lambda_1 \) and \( m \) are positive, thus

\[
\frac{d^2 I_{ref1}}{dT^2} < 0
\]

So the 1st order temperature compensation current \( I_{ref1} \) is curved-down. Similarly, we have

\[
I_{ref2} = \frac{A - BT}{R(T_0)} [1-\lambda_n(T - T_0)] + \frac{V_1 \ln N}{R(T_0)} [1 + \lambda_1(T - T_0)]
\]

(11)

Making \( dI_{ref2}/dT = 0 \), we get the ratio of \( R_a(T_0)/R_b(T_0) \):

\[
m_2 = \frac{B(1 - \lambda_n T_0) + A\lambda_n}{(1 + \lambda_1 T_0) \ln N}
\]

(12)

Differentiating Eq.(9) with respect to \( T \) gives:

\[
\frac{d^2 I_{ref2}}{dT^2} = 2(B\lambda_n + m_2\lambda_1 \frac{K}{q} \ln N) > 0
\]

(13)

From Eq.(11), we can know that the 1st order temperature compensation current \( I_{ref2} \) is curved-up.

The high order temperature compensation \( I_{REF} \) flowing through \( M_7 \) in Fig.3 is achieved by the superposition of an appropriated scaled curved-down \( I_{ref1} \) and the curved-up \( I_{ref2} \), that is:

\[
I_{REF} = AI_{ref1} + BI_{ref2}
\]

(14)

where \( A \) and \( B \) are constants defined by mirror ratios of \((W/L)_3/(W/L)_2\) and \((W/L)_5/(W/L)_6\) respectively, and \( A/B = m_2/ m_1 \).

According to analysis above, we find that the resistor tempco becomes a lovely thing, but not a boring monster.

### 3 Simulation Results and Comparison

The circuit is simulated with HSPICE and 0.6\( \mu \)m standard CMOS process model is used in the simulation.

Fig.5 and Fig.6 show the temperature dependence of \( Al_{ref1} \) through \( M_5 \) and \( Bl_{ref2} \) through \( M_6 \) at 1.8V supply, respectively. Fig.7 demonstrates the efficiency of the high order temperature compensation scheme, the achieved temperature coefficient of \( I_{REF} \) is 31 ppm/\(^\circ\)C in the temperature range of \((-50\,^\circ\)C, 100\,^\circ\)C).

According to analysis above, we find that the resistor tempco becomes a lovely thing, but not a boring monster.

From Fig.8, it is clear that the minimum supply voltage is about 1.8V, this is because the rail current source of folded-cascode goes to triode region as supply voltage below 1.8V. Nevertheless, the current changes very little with supply voltage, thus showing superior supply regulation, which is better than that achieved by the traditional cascode connection or source degeneration. Further reduction on minimum
supply voltage can be obtained by using processes with lower threshold voltage or low voltage amplifier such as bulk-driven amplifier.

Fig.9 gives the simulated PSR at 1.8 V supply without a filtering capacitor. The PSR at 10 kHz is about $-158\,\text{dB}$ and increases to $-120\,\text{dB}$ at 1 MHz. Thus the circuit shows superior power supply rejection for adopting folded-cascode amplifier. And at high frequencies, the PSR can be well improved by adding a filtering capacitor at the gate of $M_7$.

The comparison in Tab.1 shows the proposed circuit achieves better tempco with extending temperature operating range and improved line regulation.

### 4 Conclusions

A new high order temperature compensated current reference is presented in this paper. Its compensation principle is discussed and computer simulations verify the very low temperature drift. The layout of prototypes will to be considered to acquire measured results, and then trimming techniques may be necessary to guarantee the good temperature characteristic in practice for the corner of process.

<table>
<thead>
<tr>
<th>Tab.1 Comparison of Simulation Results Current References</th>
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<tr>
<td>Min.$V_{\text{DD}}$/V</td>
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<tr>
<td>-----------------------</td>
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<tr>
<td>Tempco /ppm/(°C)$^{-1}$</td>
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<tr>
<td>Line regulation /V</td>
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<td>PSR/dB</td>
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<tr>
<td>Temperature range /°C</td>
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### References


### Brief Introduction to Author(s)

ZHOU Hao (周浩) was born in Anhui, China, in 1982. He is pursuing the M.S. degree at University of Electronic Science and Technology of China (UESTC). His main research interests include low-voltage, low-power amplifiers, current reference and voltage reference.

ZHANG Bo (张波) was born in 1964. Now he is professor and doctoral advisor with UESTC. His research interests include power devices and smart power ICs.

LI Zhao-ji (李昭基) received the B.S. degree from Chengdu institute of Radio Engineering in 1963. Now He is professor and doctoral advisor with UESTC. His research interests include power devices and smart power ICs.

LUO Ping (罗萍) received his doctoral degree from UESTC in 2004. Now she is vice professor, her research interests include SMPS modelling and smart power ICs.